



IC55H-A v:1.0

(LGA1156P Processor with DDR3 SDRAM Mainboard)

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REVISION HISTORY:

Rev	Date	Notes
A	2010.01.29	INITIAL RELEASE
1.0	2010.04.26	INITIAL RELEASE

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

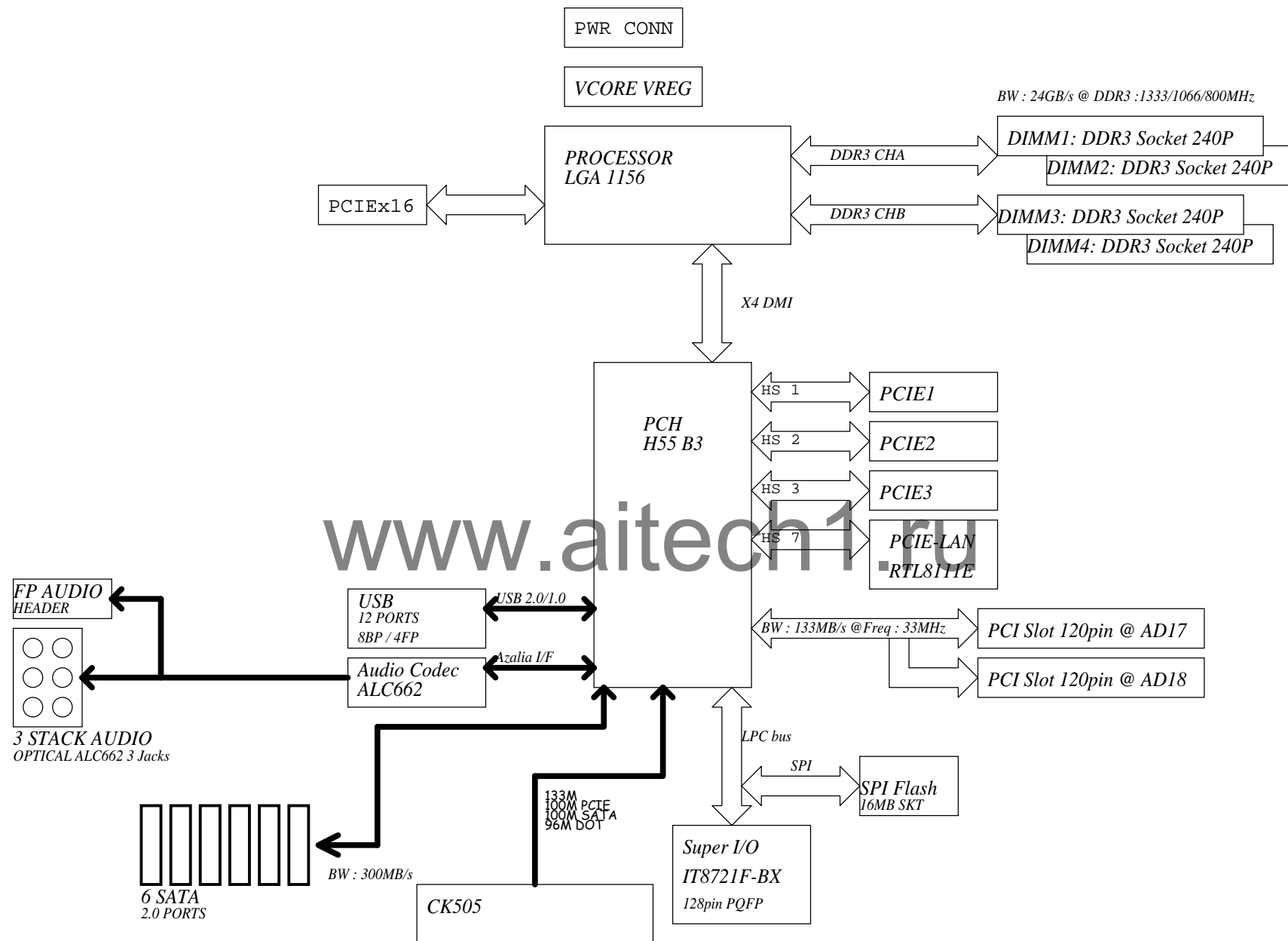


3) DESIGN NOTES in red are critical, and must be understood and followed.

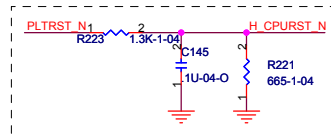
PCB STACK: L1:TOP
L2:VCC
L3:GND
L4:BOTTOM


Elitegroup Computer Systems			
Title Cover Page			
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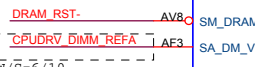
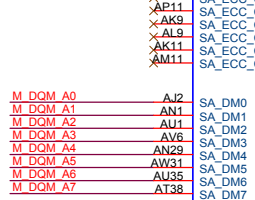
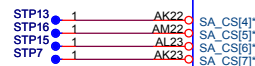
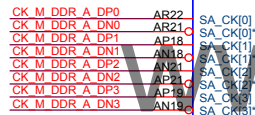
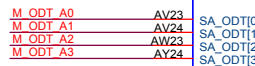
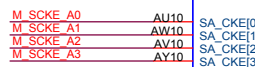
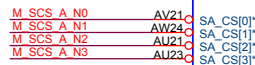
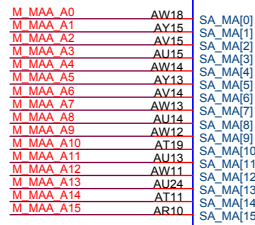
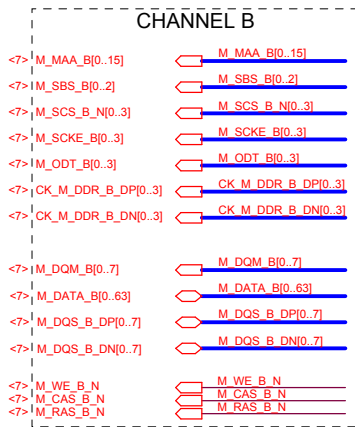
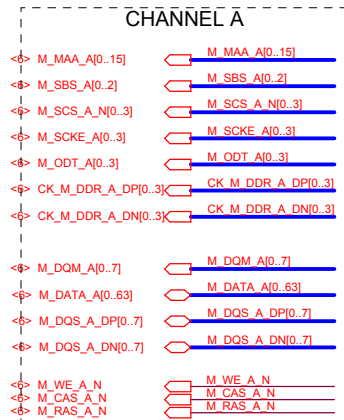
PCB : 305 x 210 mm ; 4 layers



CPUD

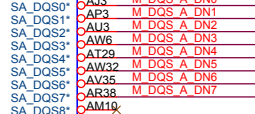
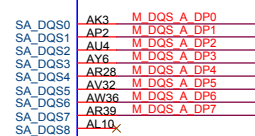
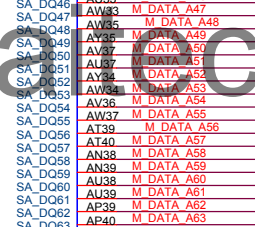
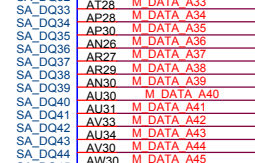
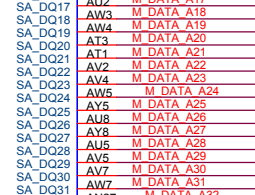
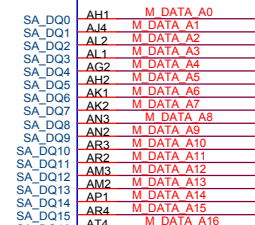


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Title LGA1156 CPU/GPU/PEG/DMI			
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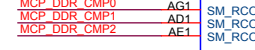
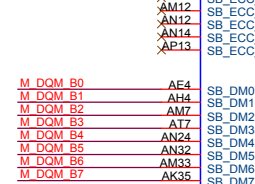
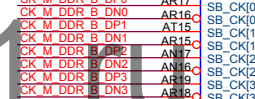
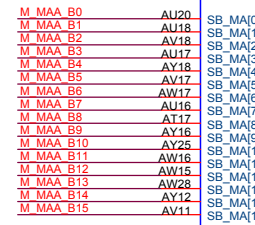


LGA-1156P-S

1 OF 7



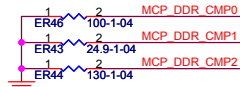
LGA-1156P-S



CPUDRV_DIMM_REFB AG3 SB_DM_VREFDQ

LGA-1156P-S

2 OF 7

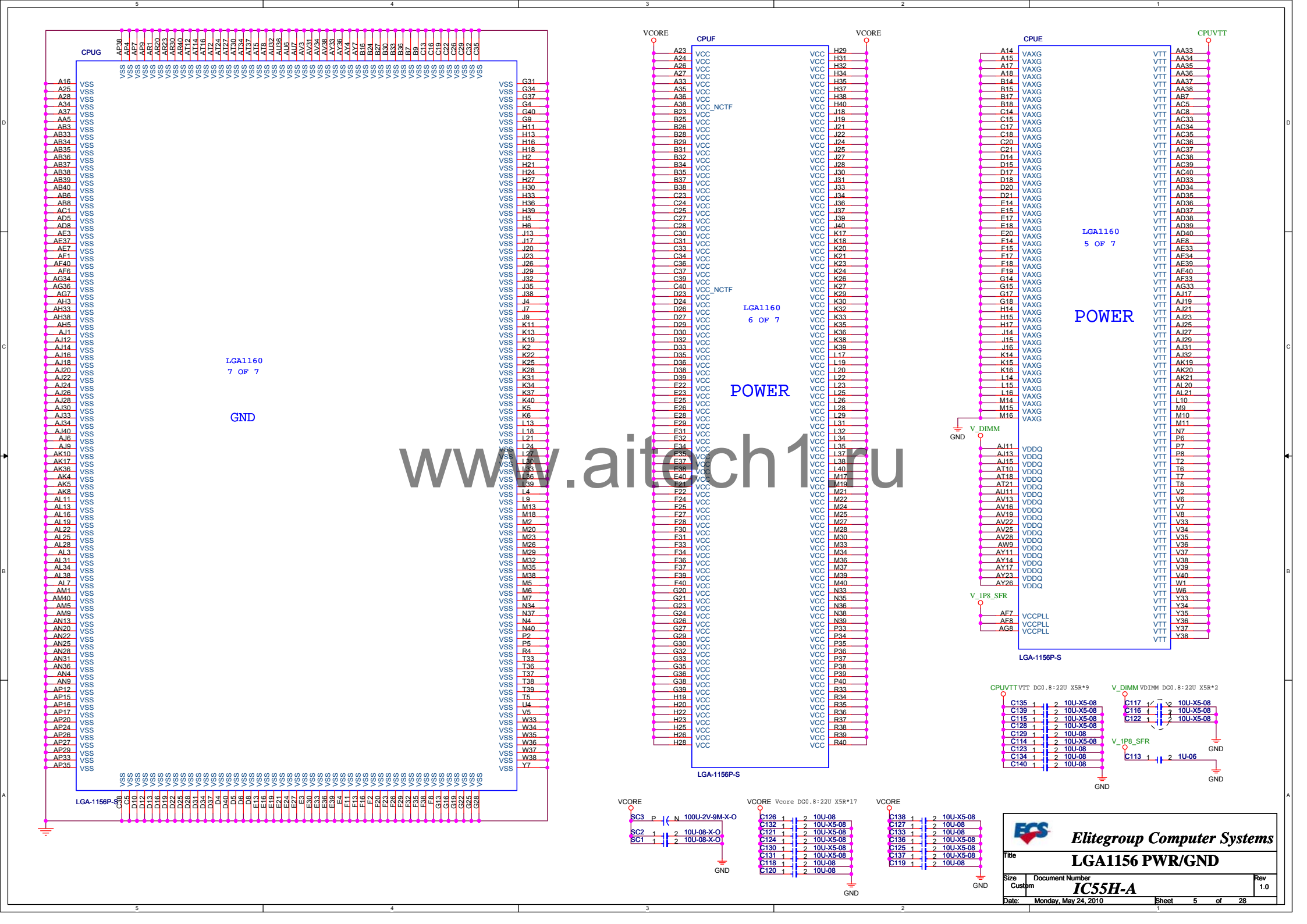


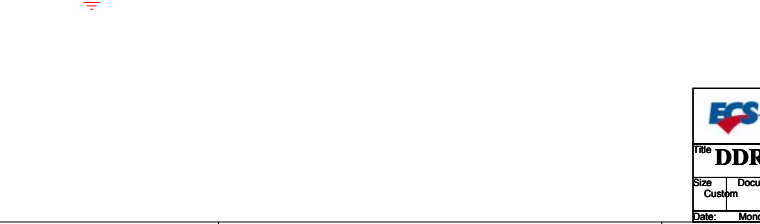
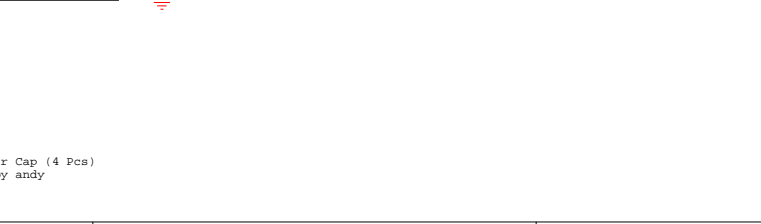
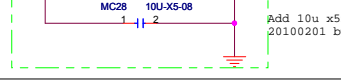
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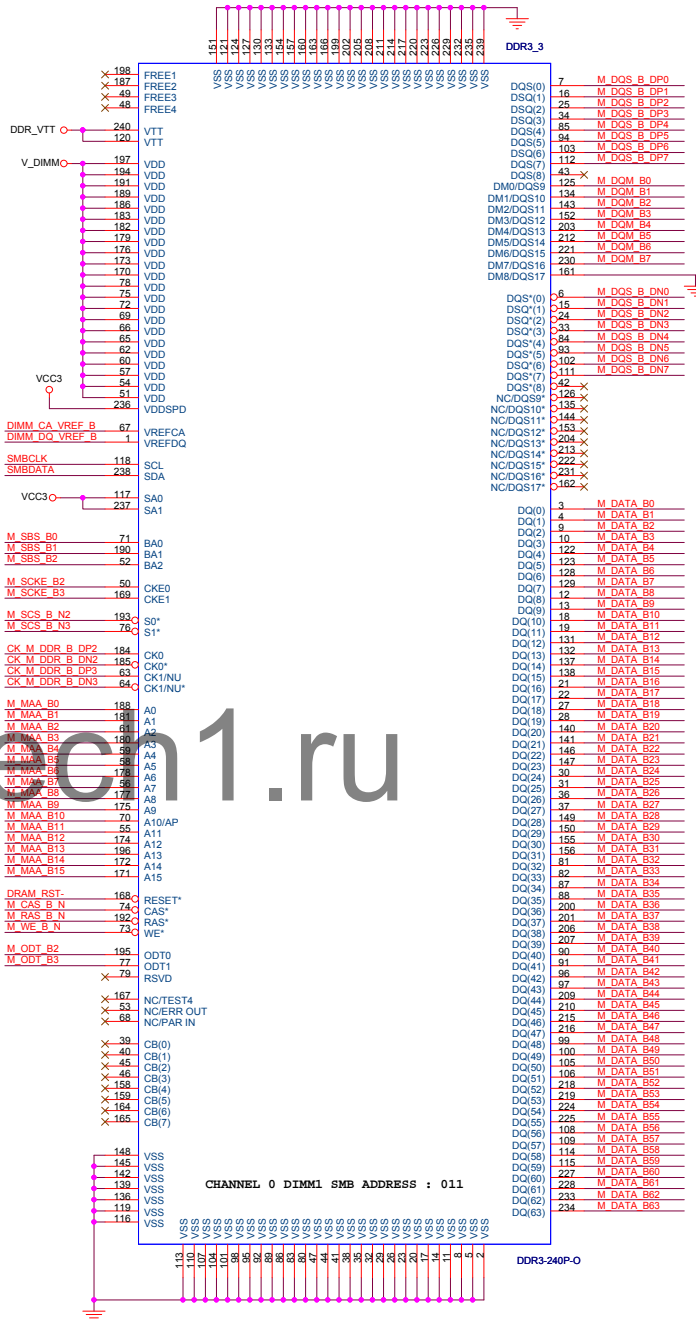
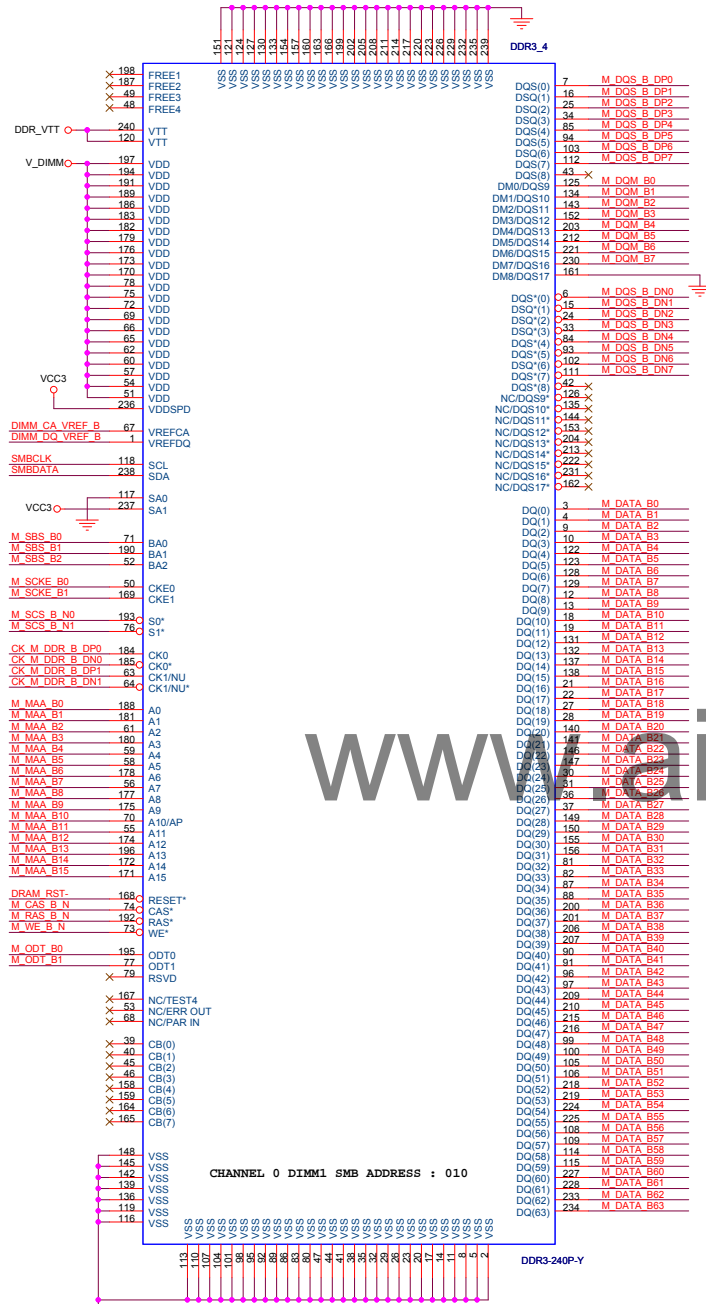
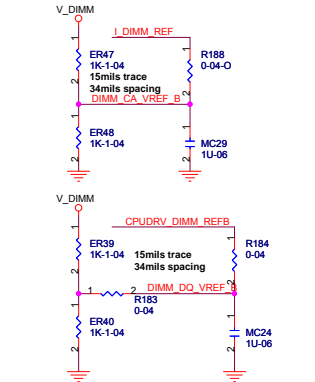
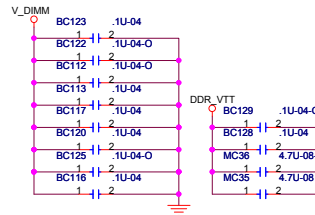
Title LGA1156 DDR3 MEMORY

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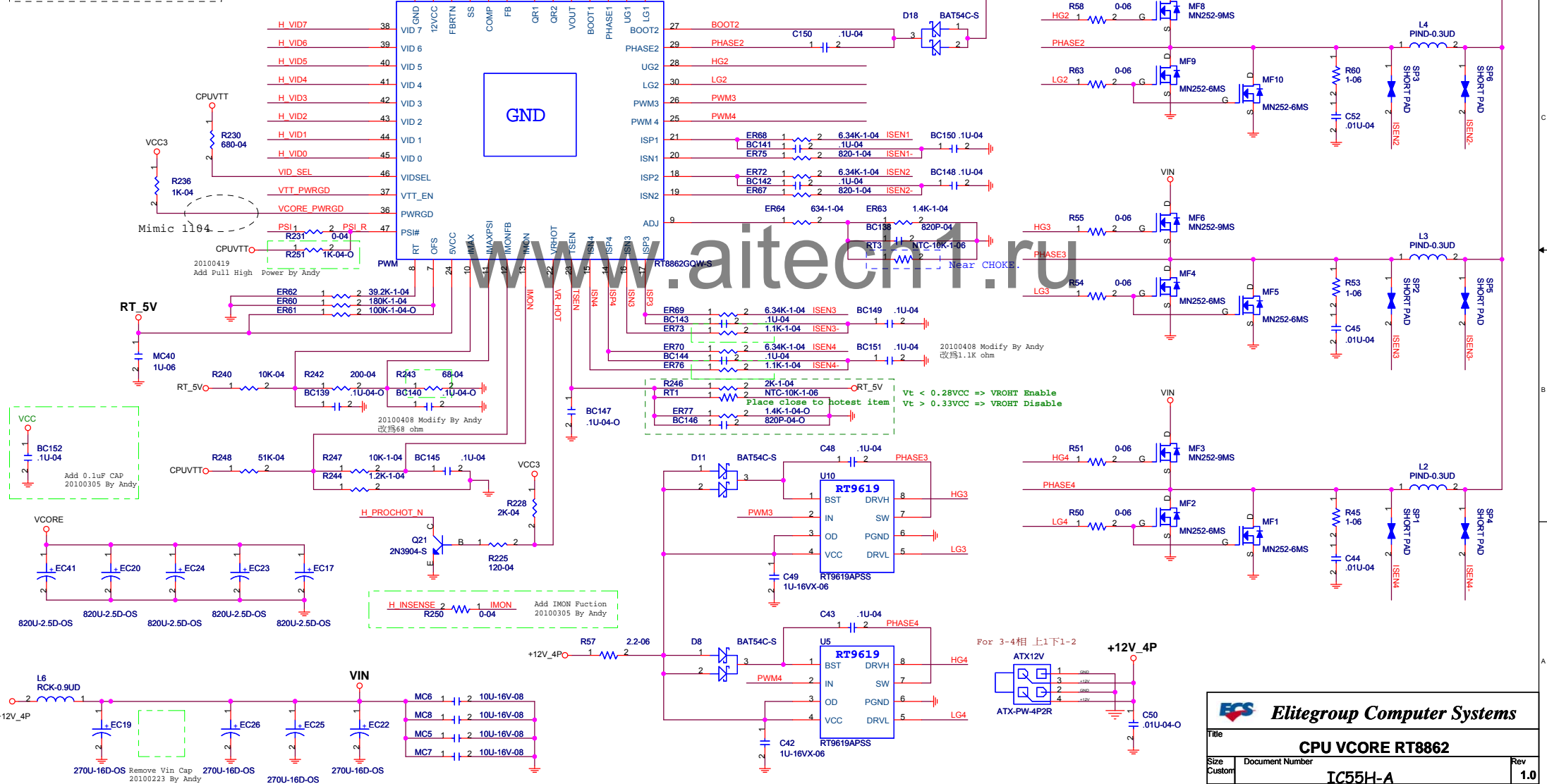


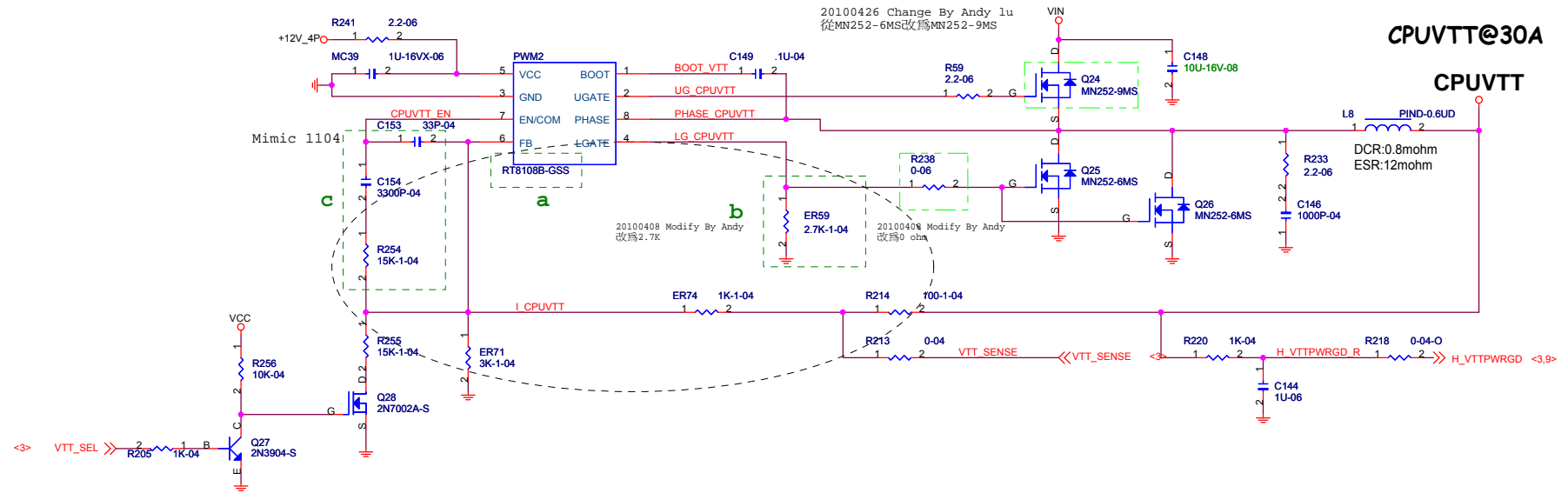


[illegible]

VCC VCORE CPUVTT

H_VID[0..7] VCC_SENSE VSS_SENSE VTT_PWRGND VCORE_PWRGND VCORE_FB H_INSENSE H_PROCHOT_N PSI





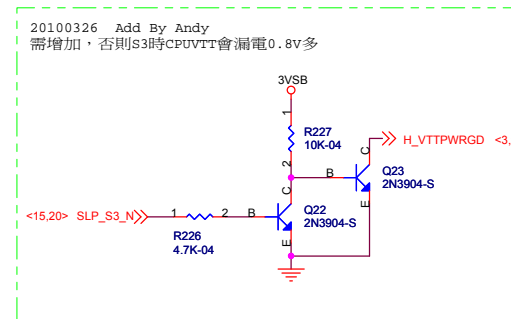
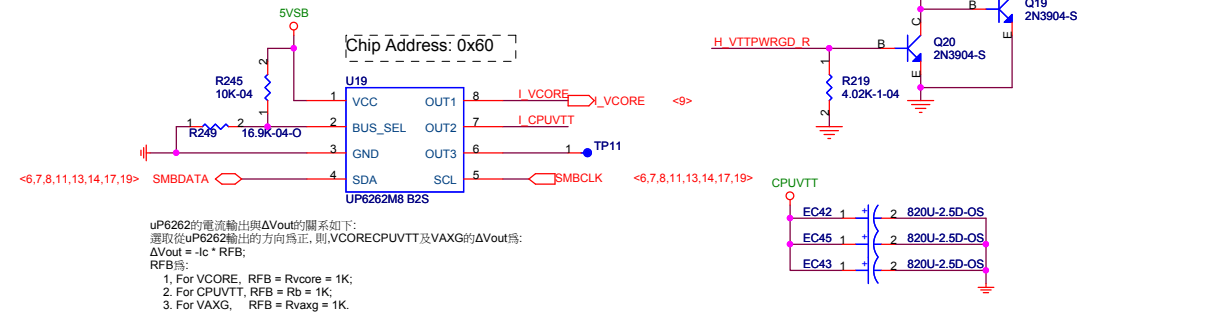
VTT_SEL	CPUVTT
1	1.05V
0	1.10V

OCP : 40A

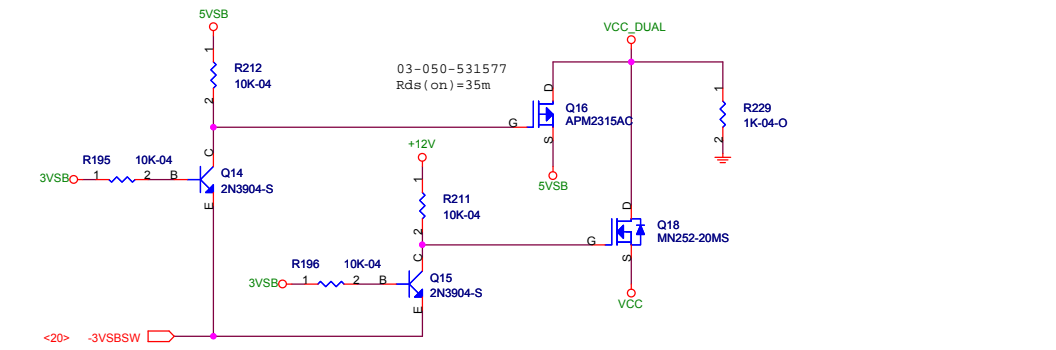
$$I_{ocp} = \frac{50u * R_{oc}}{R_{ds(on)}}$$

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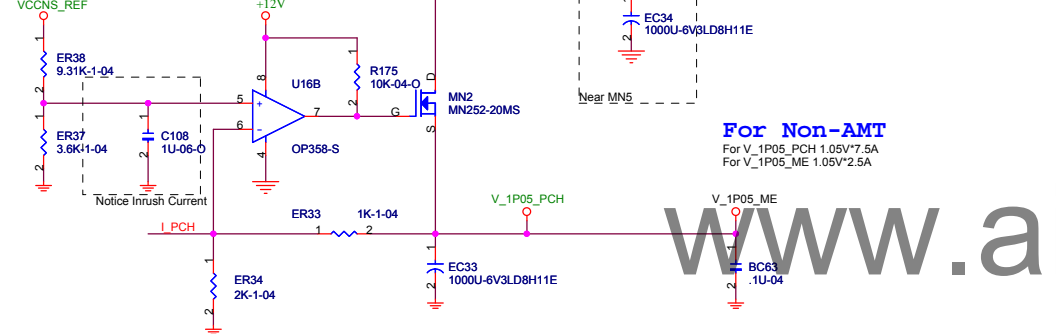
	UPI 30A	Richtek 30A
a	UP6109ASA8S	RT8108BGS
b	10K-1-04	2.4K-1-04
c	X	O



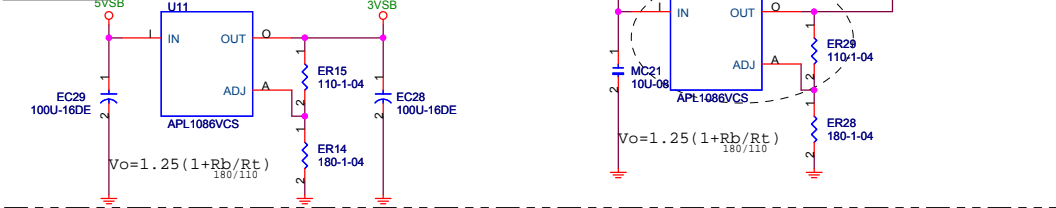
VCC_DUAL



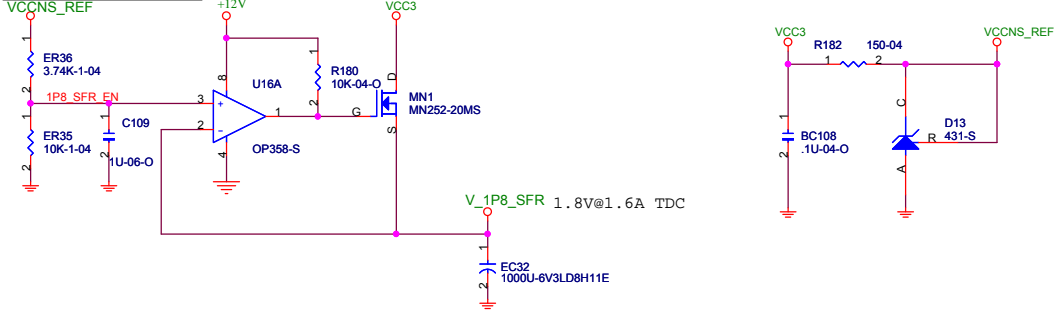
PCH Core



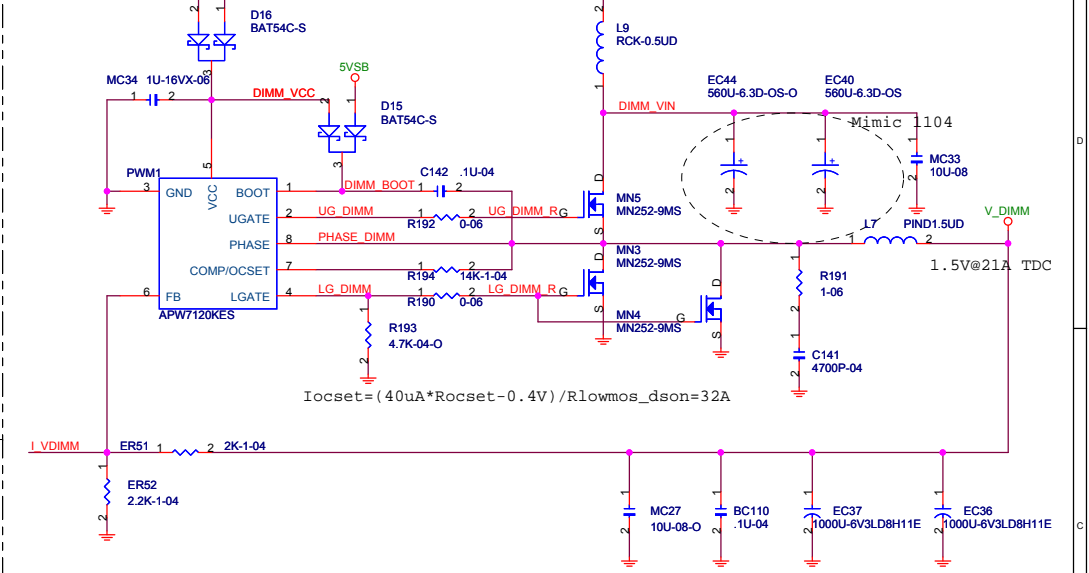
3VSB



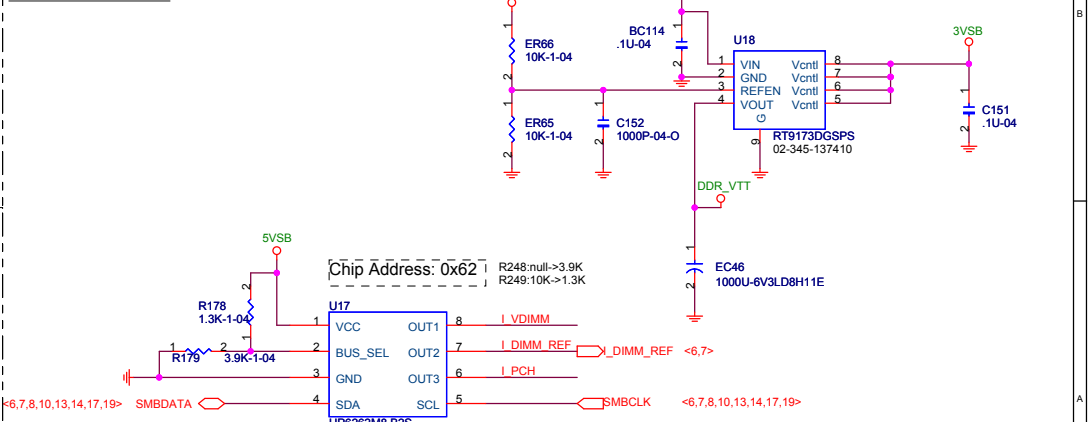
V_1P8_SFR



V_DIMM

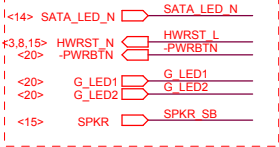


DDR_VTT

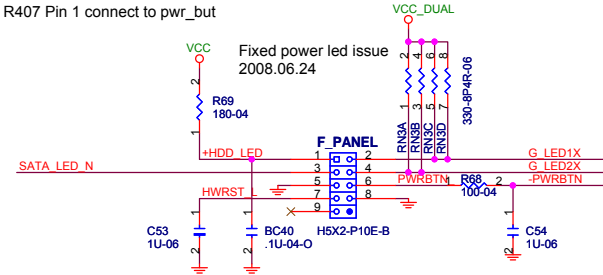


FRONT PANEL

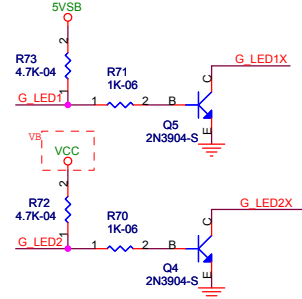
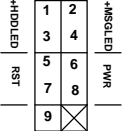
External Connection



R407 Pin 1 connect to pwr_but



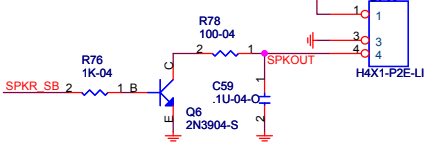
F_PANEL



S0	S1	S3	S4	S5
G_LED1	B	B	L	L
G_LED2	H	L	L	L
B	SB	YB	OFF	OFF

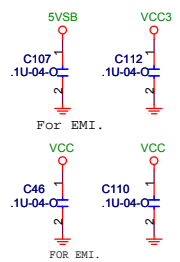
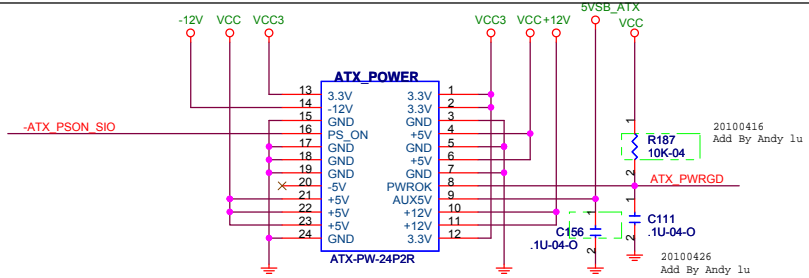
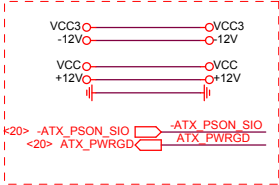
B: Blinking

BUZZER SPK Colay



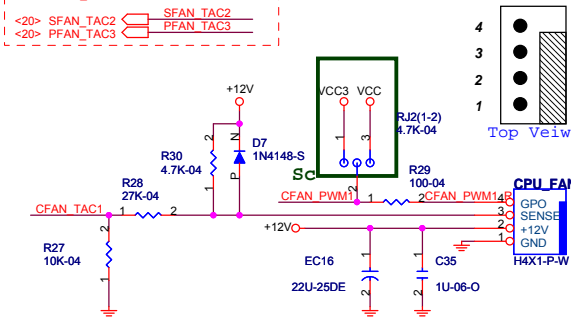
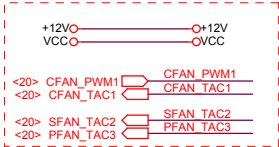
POWER CONNECTOR

External Connection

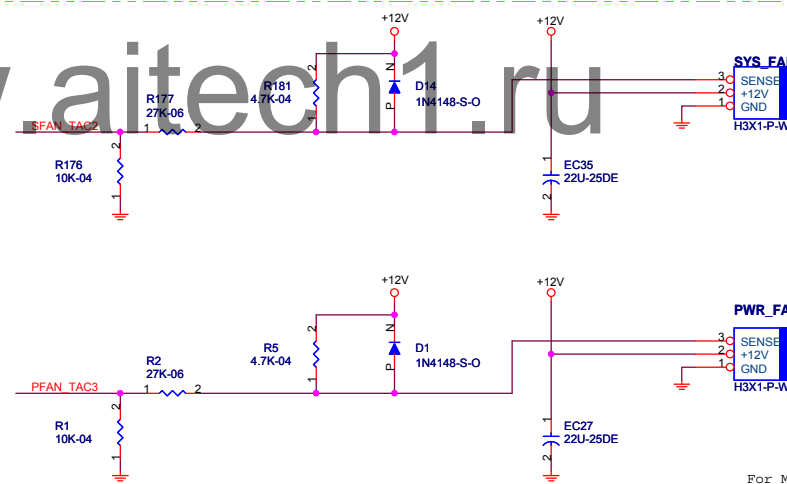


FAN

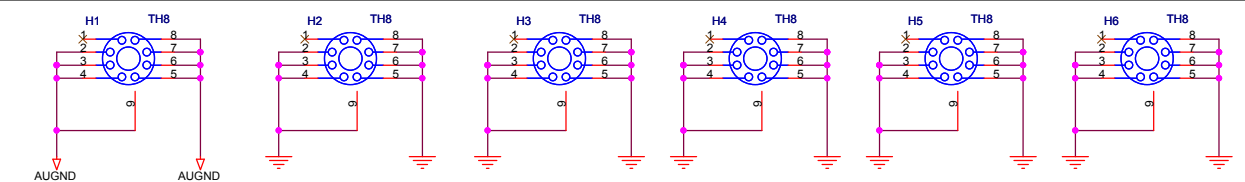
External Connection



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For MRS Update
20100204 by andy



Title
Front Panel,FAN,PowerConn

Size
Custom

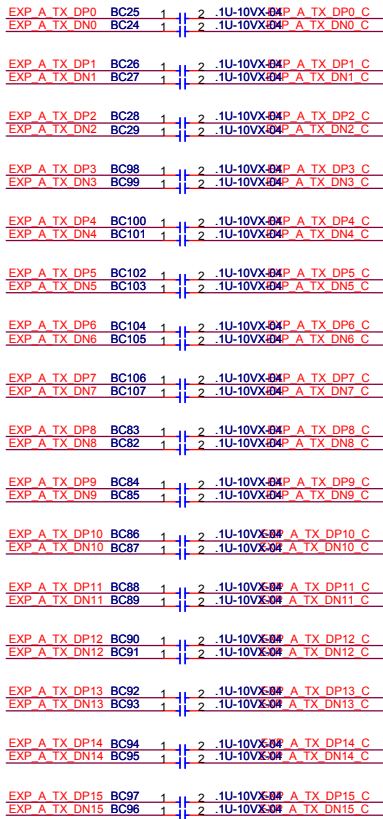
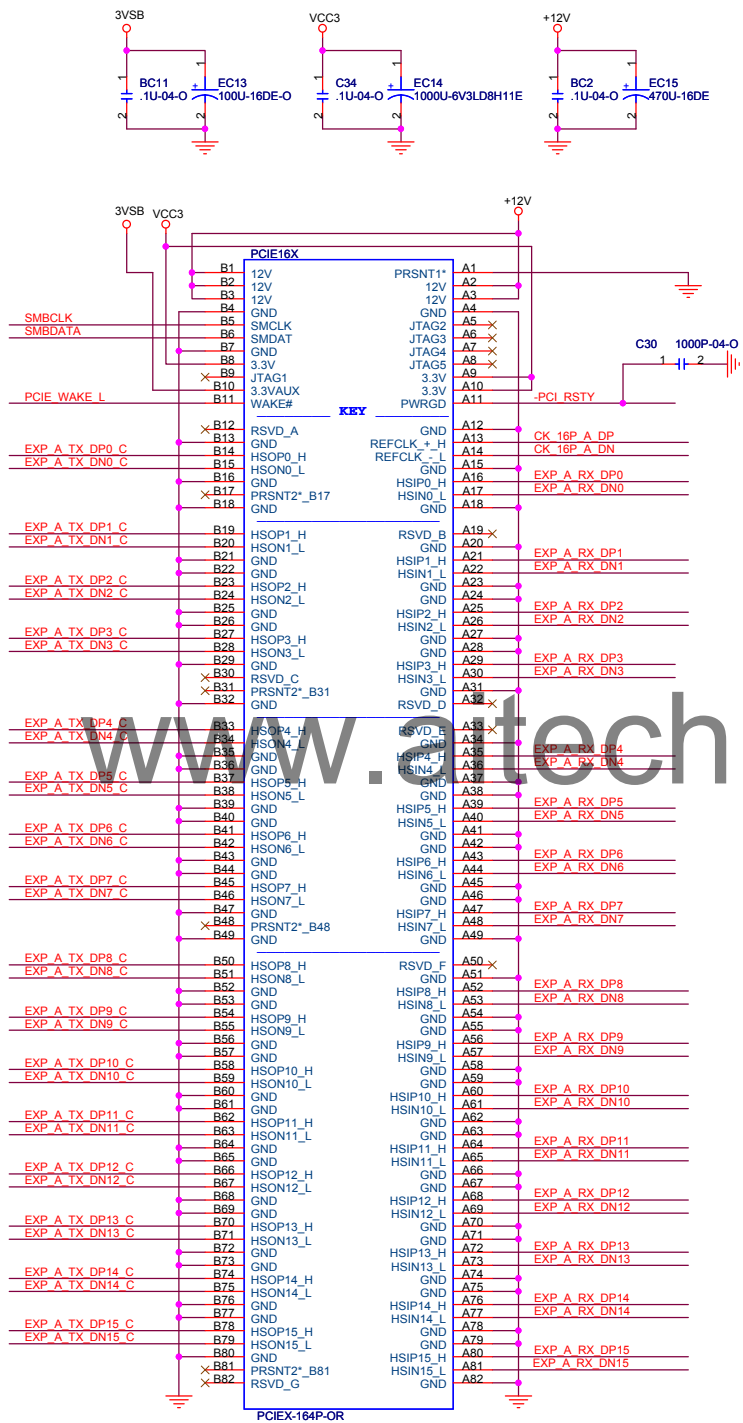
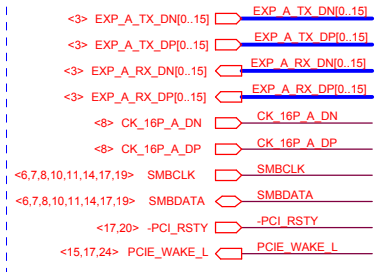
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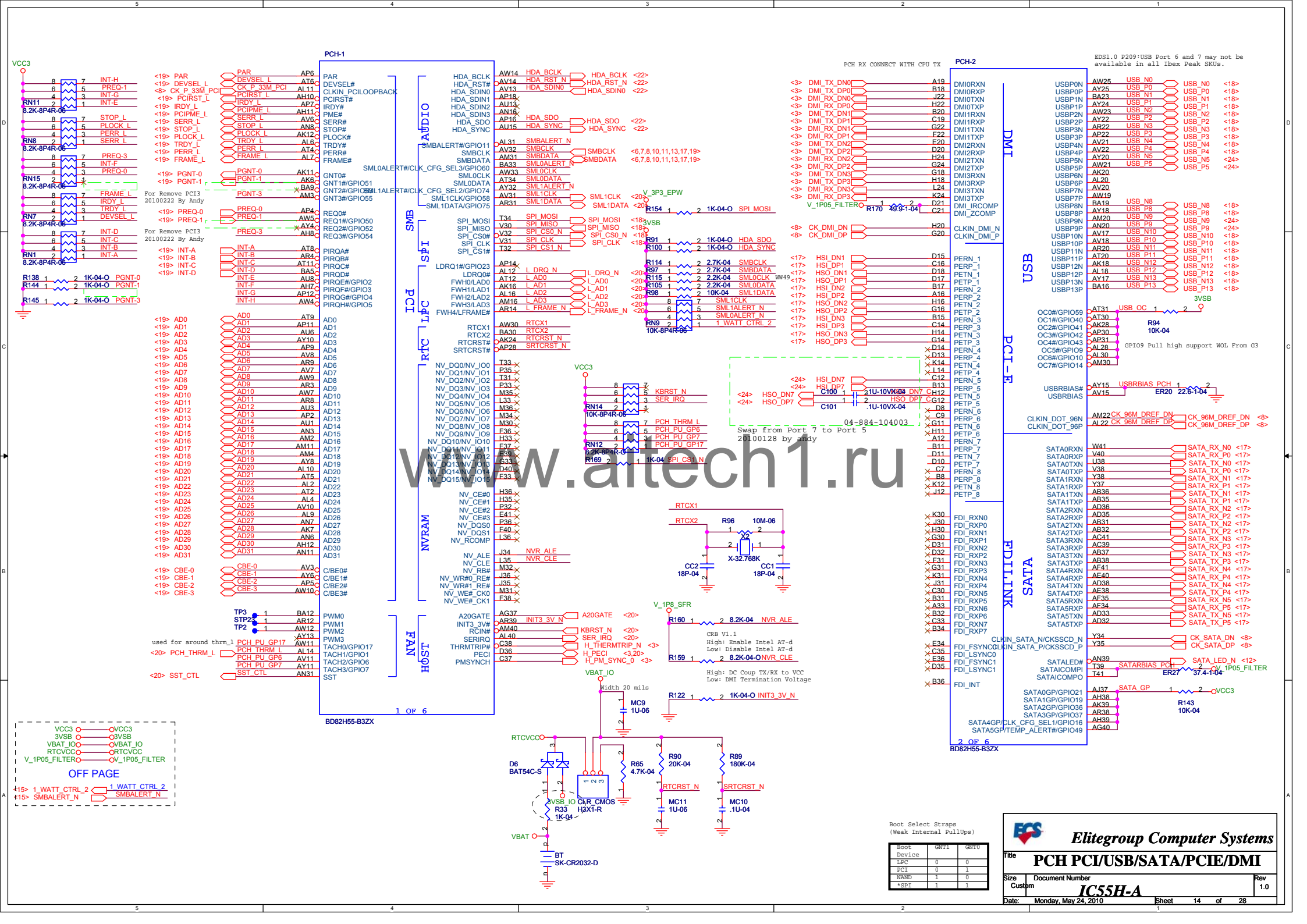
PCIEX16



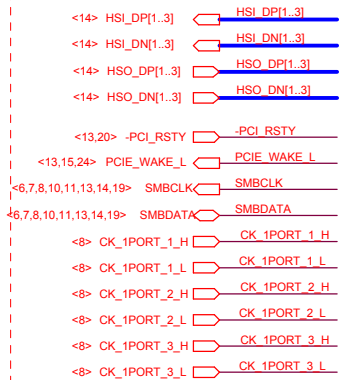
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Cap改為X7R

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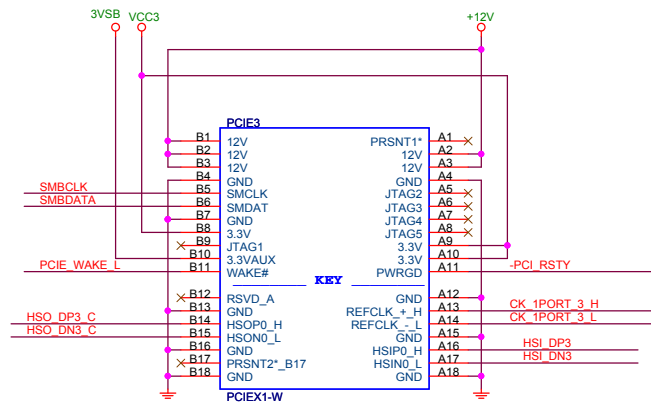
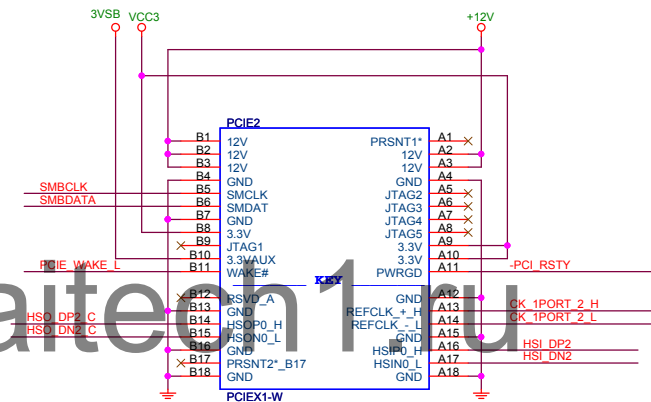
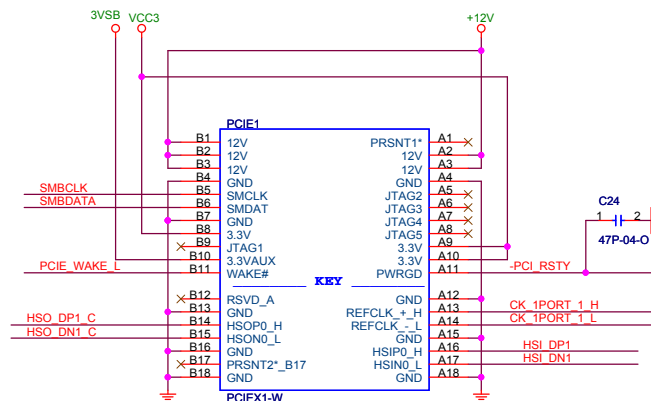
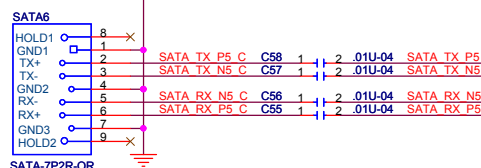
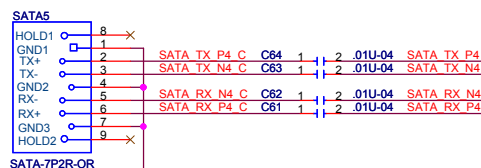
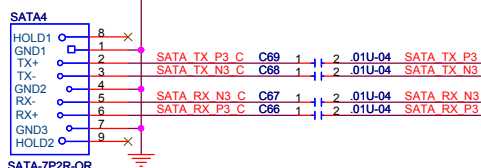
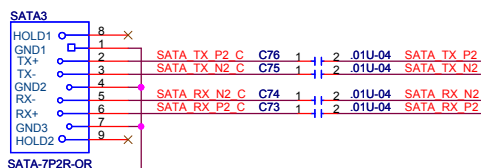
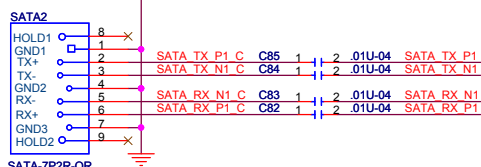
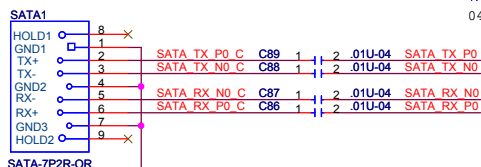
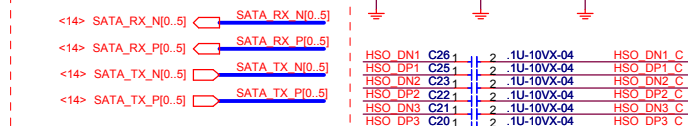
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Size	Document Number	Rev			1.0
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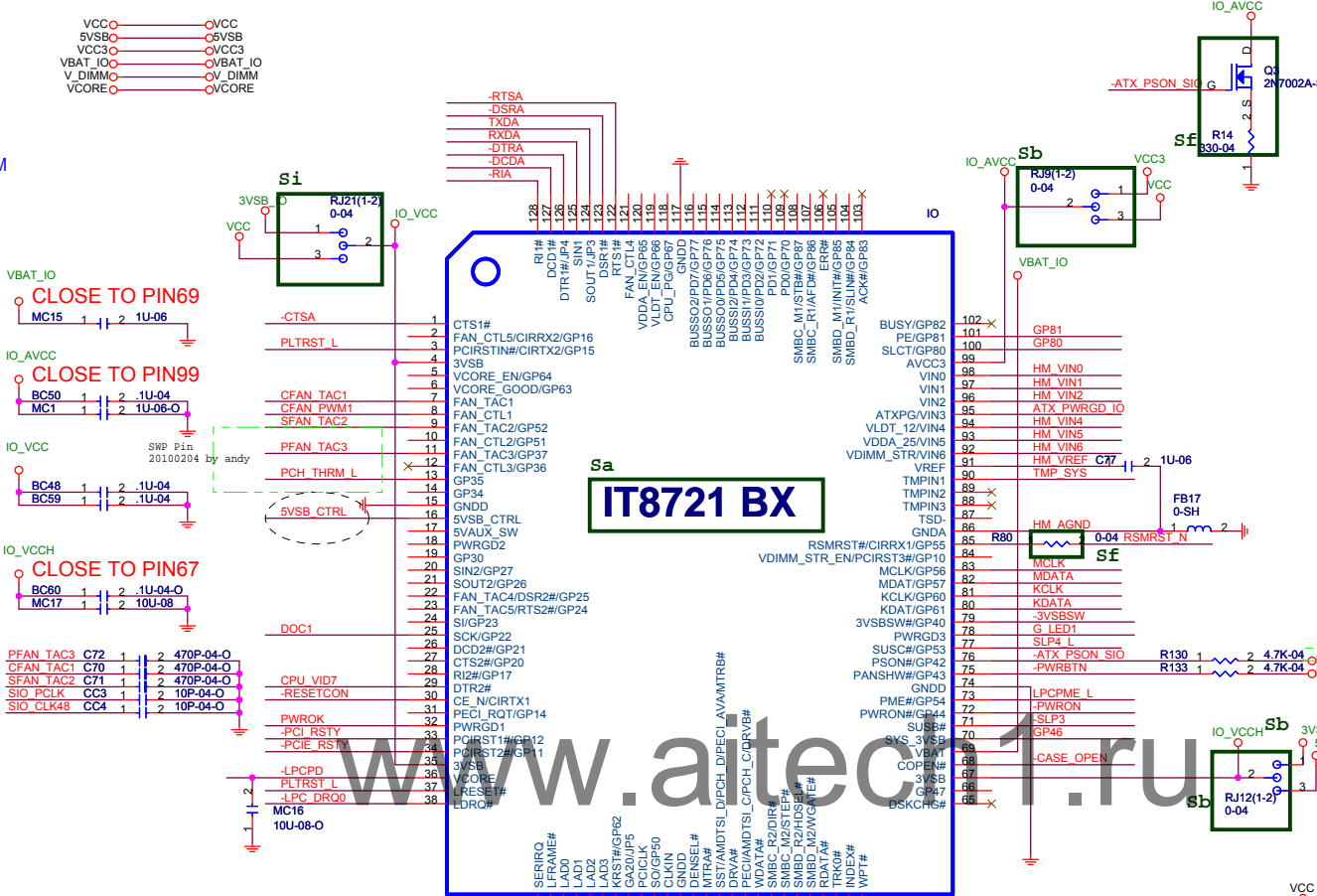
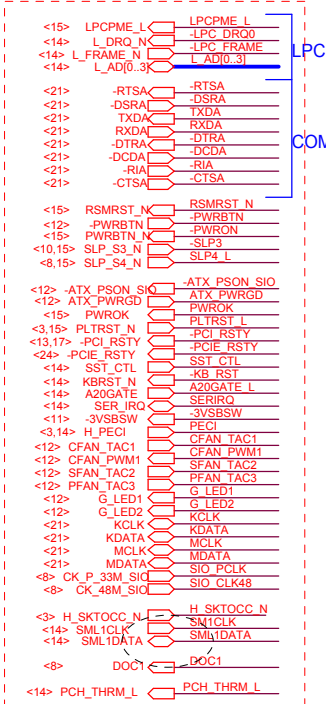
External Connection



External Connection



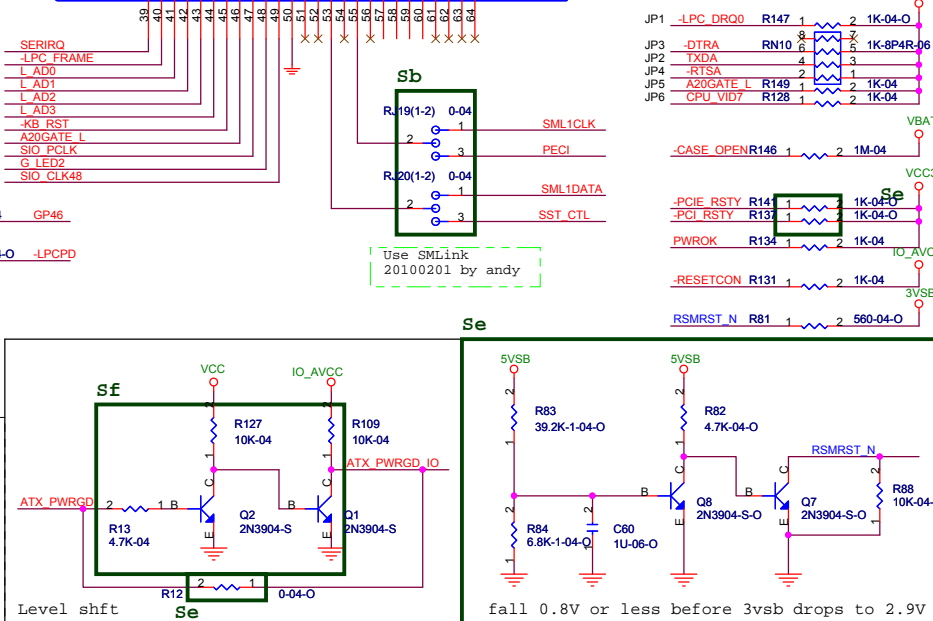
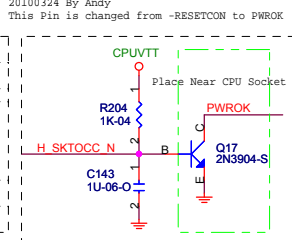
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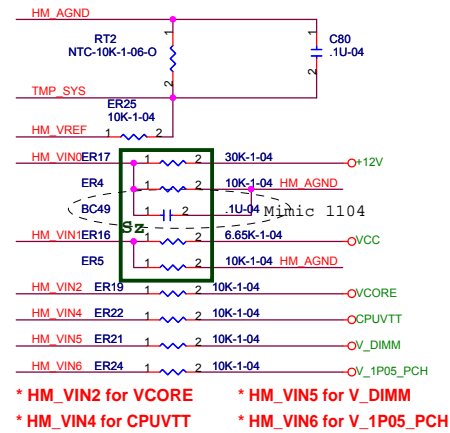
	IT8720 JX	IT8721 CX	IT8721 BX
sa	IT8720 JX	IT8721 CX	IT8721 BX
sb	(2-3)	(1-2)	(1-2)
sc	(2-3)	(1-2)	(1-2)
sd	X	X	0-04
se	V	X	X
sf	X	V	X
sh	V	V	X
sq	X	X	V
sz	X	X	V

HW STRAPPING

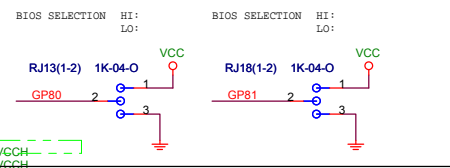
UP1 Pin 38	FlashSeg1_EN	0	Disabled.
JP2 Pin 122	VIDO_EN	0	Disable VID output pins
JP3 Pin 124	CHIP_SEL	0	Chip selection in Configuration
JP4 Pin 126	K8PWR_EN	1	K8 power sequence function is disabled
UP3 Pin 124	FAN_CTL_SEL	0	The default value of EC index 15h/16h/17h is 00h
UP5 Pin 46	WDT_EN	0	The default value of EC index 15h/16h/17h is 20h
JP5 Pin 46	WDT_EN	0	The default value of EC index 15h/16h/17h is 7fh
UP6 Pin 29	SVID_EN	0	Disable WDT to rest PWROK
		1	Enable WDT to rest PWROK
		0	Disable SVID Function
		1	Enable SVID Function



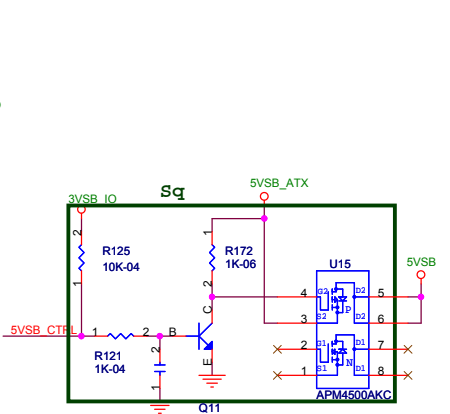
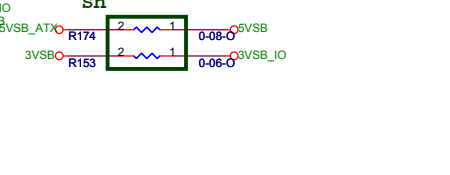
Thermal and Voltage Monitor



BIOS SELECTION



EUP



LPC SIO-ITE8720

Title	LPC SIO-ITE8720	
Size	Document Number	IC55H-A
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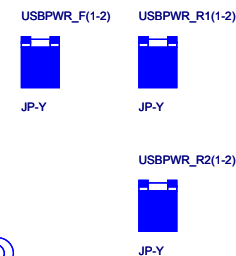
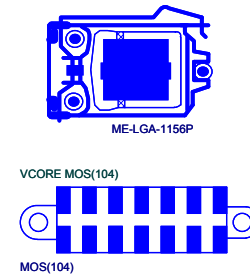
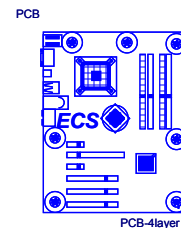
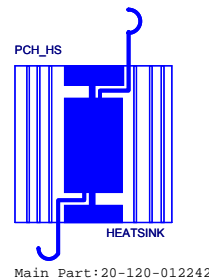
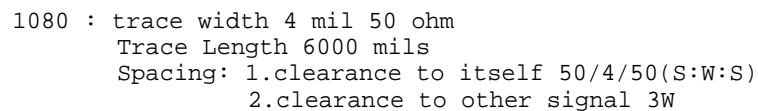


Diagram showing the pin connections for the PCH_RI_PU module. The module has 16 pins, numbered 1 to 16. The connections are as follows:

- Pin 1: +12V
- Pin 2: VCC
- Pin 3: -12V
- Pin 4: -RIA
- Pin 5: -DTRA
- Pin 6: -CTSA
- Pin 7: TXDA
- Pin 8: -RTSA
- Pin 9: RXDA
- Pin 10: -DSRA
- Pin 11: -DCDA
- Pin 12: RIA
- Pin 13: DTRA
- Pin 14: CTSA
- Pin 15: TXDA
- Pin 16: RTSA

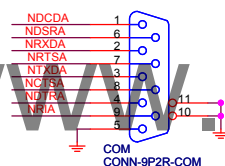
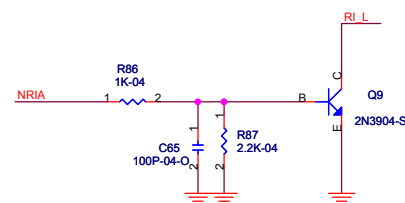
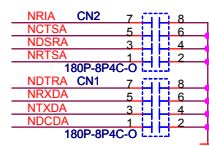
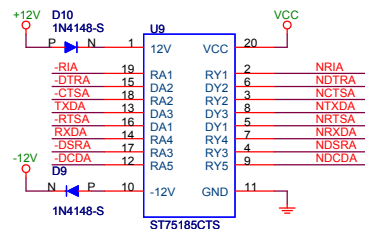
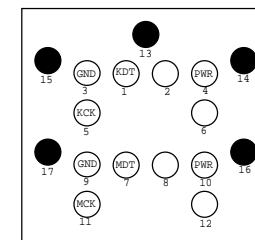
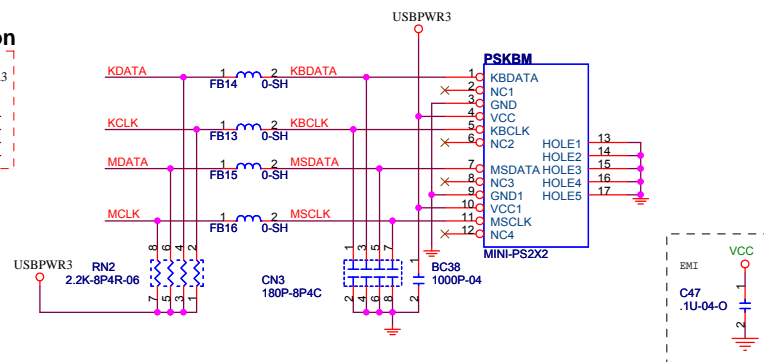


Diagram illustrating a 10-bit bus system. The bus consists of 10 data lines (NDSRA, NRXDA, NRTSA, NITXA, NCTSA, NUTRA, NUTRA, NUTRA, NUTRA, NUTRA) and 2 control lines (C10, C11). The bus is connected to a 10-bit bus system.

USBPWR3 ○ ——— ○ USBPWR3

<20>	KDATA	KDATA
<20>	KCLK	KCLK
<20>	MDATA	MDATA
<20>	MCLK	MCLK



5VSB

3VSB

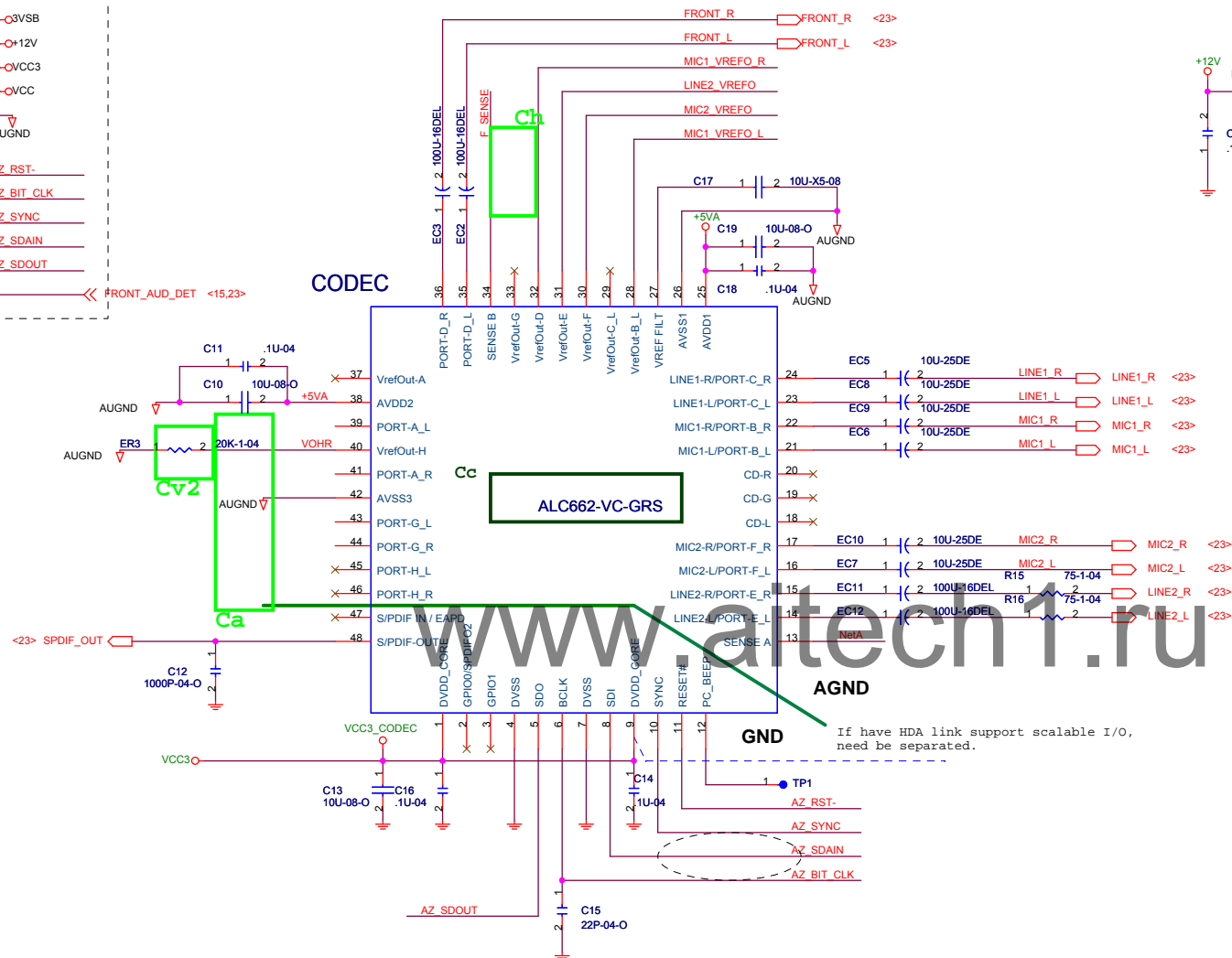
+12V

VCC3

VCC

AUGND

AUGND

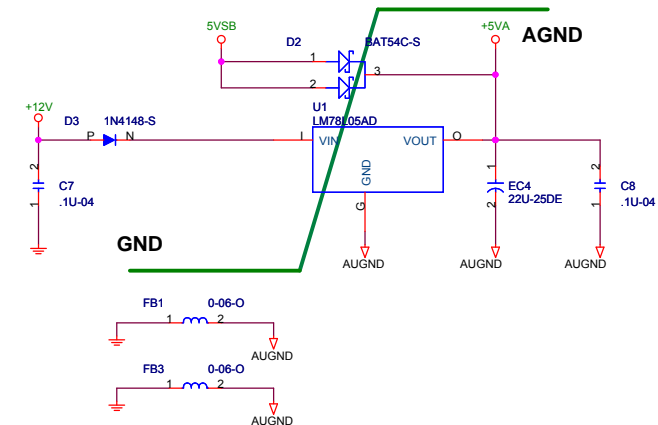


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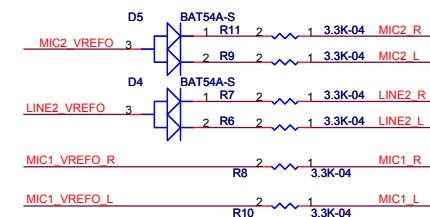
Location	ALC888VC 7.1 Ch	ALC662 5.1 CH	VT1705B 5.1CH	VT1818S 7.1CH	VT1828S 7.1CH
Ca	V	X	X	V	V
Cc	ALC888-GR C2S	ALC662-VC-GRS	VT1705BS	VT1705BS	VT1705BS
Cd	V	X	X	V	V
Ce	AUDIO-26P-LOT	AUDIO-3P-HDA	AUDIO-3P-HDA	AUDIO-3P-HDA	AUDIO-3P-HDA
Cf	V	X	X	V	V
Cg	V	X	X	V	V
Ch	V	X	X	X	X
Cv1	RJ2(1-2)	RJ2(1-2)	RJ2(2-3)	RJ2(2-3)	RJ2(2-3)
Cv2	20K-1-04	20K-1-04	5.1K-1-04	5.1K-1-04	5.1K-1-04

```
Pin2
VT1705 : SPDIFO2/GPIO1
VT1708 : SPDIFO2
VT1818 : DIMIC_CLK
```

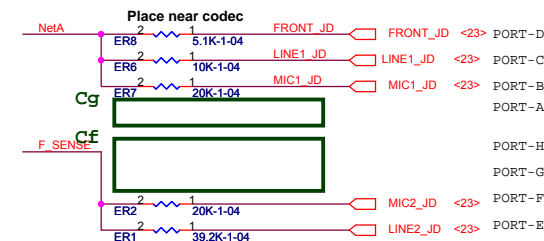
```
Pin3
VT1705 : GPIO2
VT1708 : SPDIFI2
VT1818 : DMIC_DATA
```



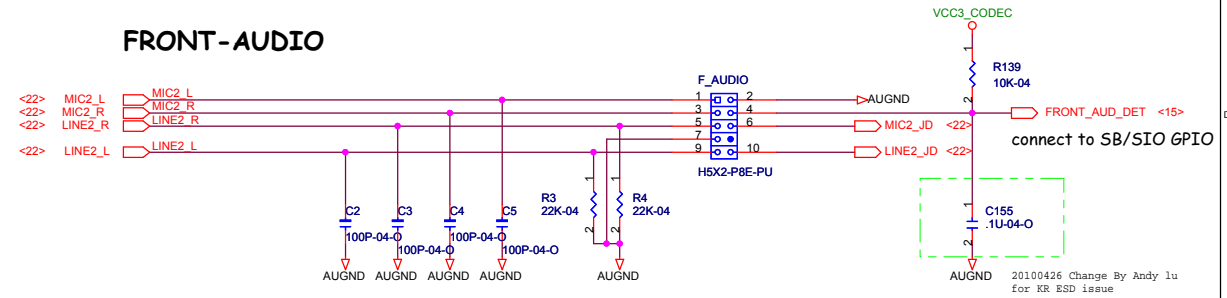
Verfout bias for stereo microphone.



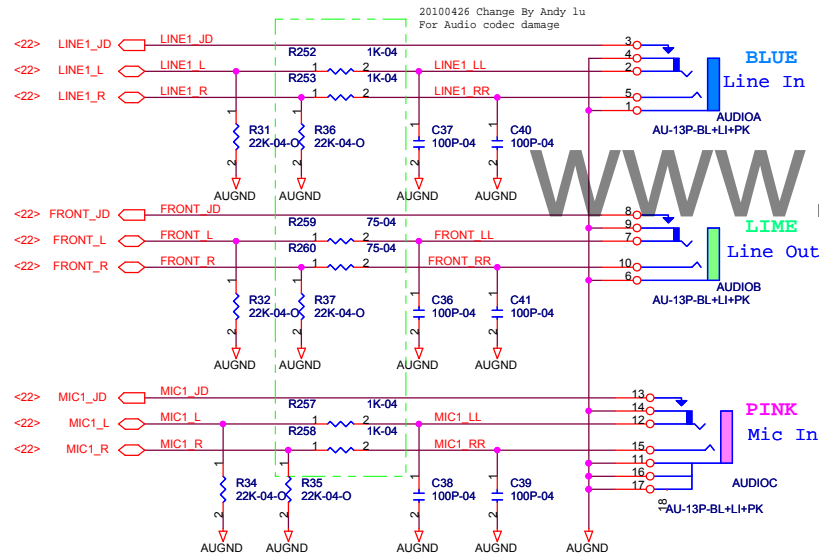
Place near Chip



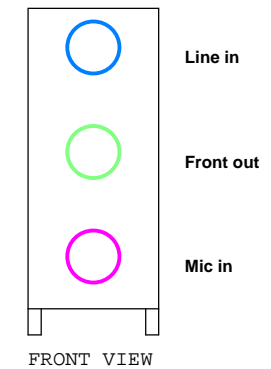
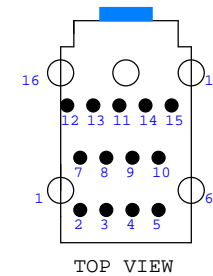
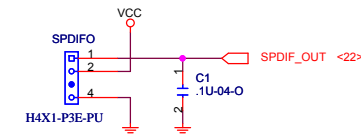
FRONT-AUDIO



REAR-AUDIO



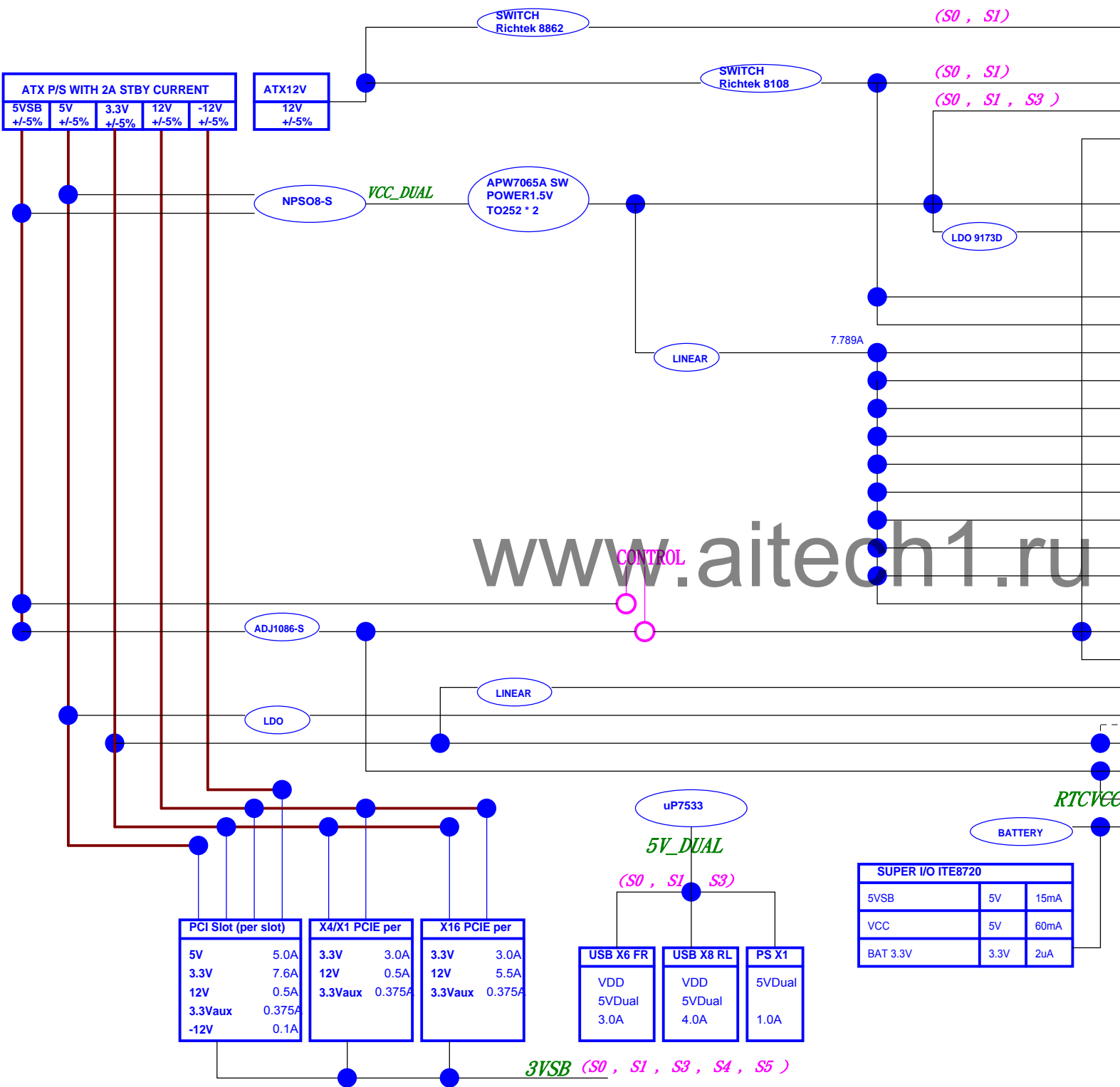
SPDIF-OUT



Elite **ECS** Computer Systems

Title **Audio Connector**

Size	Document Number	Rev
Custom	IC55H-A	1.0
Date:	Monday, May 24, 2010	Sheet 23 of 28



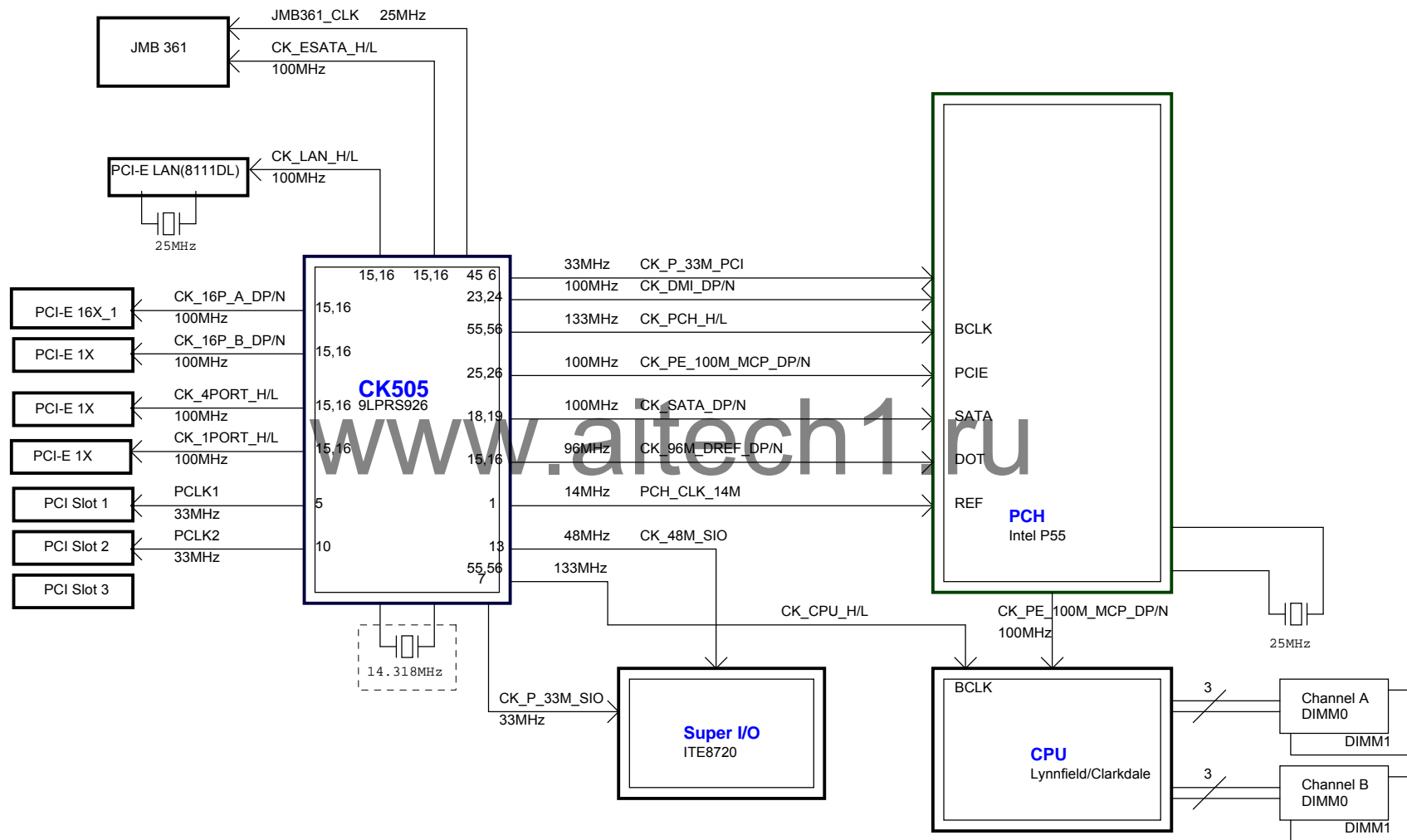
Intel Lynnfield/Havendale CPU		
VCORE	VID 0.65~1.4	90A/110A
VAXG	VID 0.8~1.3	16A/20A
CPUVTT	1.05~1.1	30/35A
V_DIMM	1.5V	2.8/6A
V_1P8_SFR	1.8V	0.8/1.1A

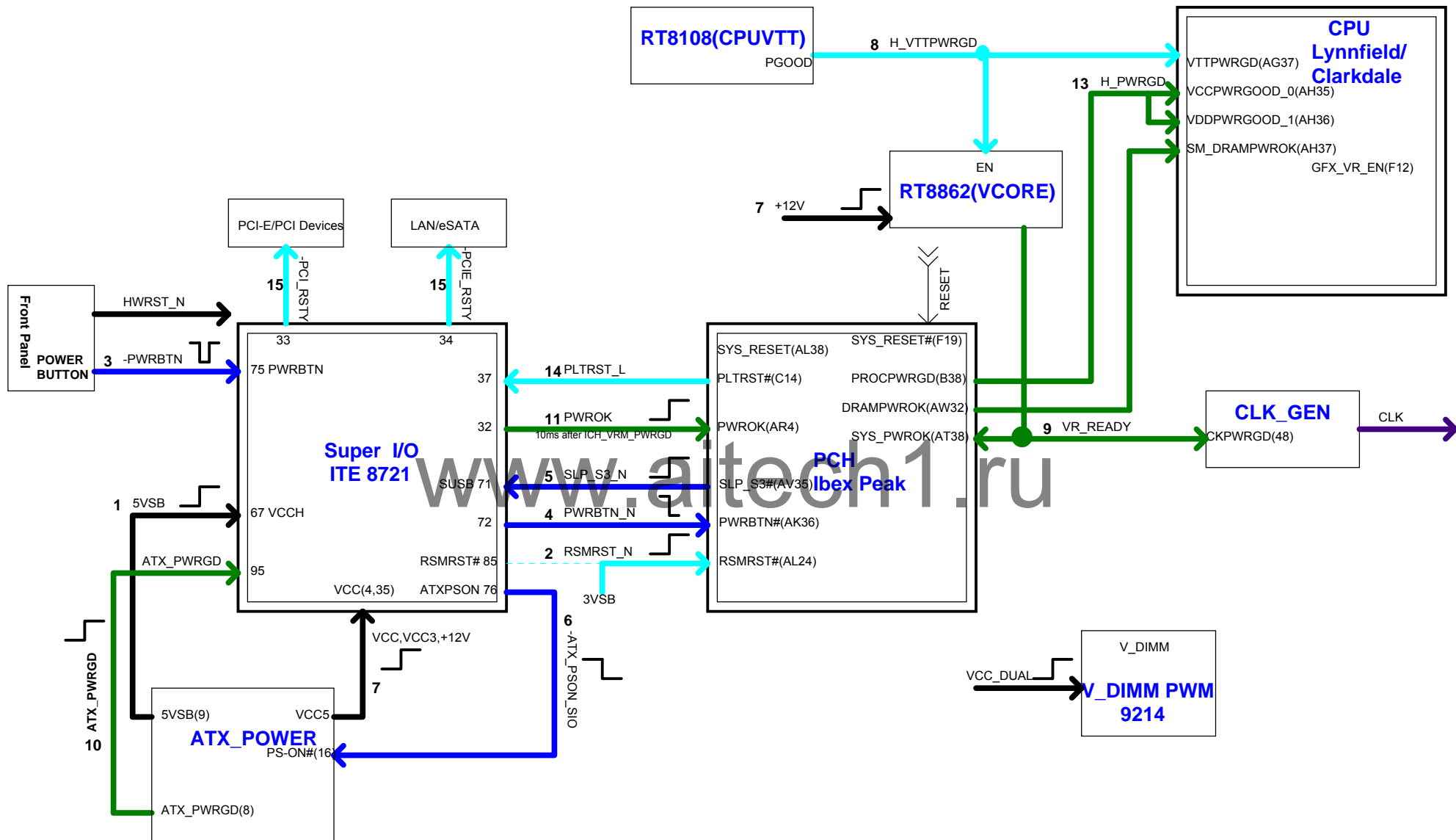
DDR3 4DIMMs		
V_DIMM	1.5V	7.2A
DDR_VTT	0.75V	1A

Intel PCH		
VCCDMI	1.1V	0.065A
V_CPU_IO	1.05/1.1V	<1mA
VCC_CORE	1.05V	1.629A
VCCIO	1.05V	3.251A
VCCLAN	1.05V	0.372A
VCCADPLLA	1.05V	0.075A
VCCADPLLB	1.05V	0.075A
VCCACLK	1.05V	0.052A
VCCSATAPLL	1.05V	0.031A
VCCAPLLEXP	1.05V	0.045A
VCCFDIPLL	1.05V	0.037A
VCCME	1.05V	2.222A
VCCVRM	1.8V	0.043A
VCCPNAND	1.8V	0.156A
VCCME3_3	3.3V	0.086A
VCCADAC	3.3V	0.069A
VCC3	3.3V	0.357A
VCCSUS3_3	3.3V	0.168A
VCCSUSHDA	3.3V	0.006A
RTCVCC	3.3V	0.002A

SUPER I/O ITE8720		
5VSB	5V	15mA
VCC	5V	60mA
BAT 3.3V	3.3V	2uA

AZALIA		
DVDD	3.3V	40mA
AVDD	5V	51mA





PCH STRAPS TABLE															
	H	L	DESCRIPTION												
PGNT-3	(inter pu)	*Top Boot Block(-0)	A16 SWAP OVERRIDE Low: OVERRIDE												
PGNT-1, PGNT-0	<table border="1"><tr><td>BOOT DEVICE</td><td>GNT0</td><td>GNT1</td></tr><tr><td>LPC</td><td>0</td><td>0</td></tr><tr><td>PCI</td><td>0</td><td>1</td></tr><tr><td>*SPI</td><td>1</td><td>1</td></tr></table>	BOOT DEVICE	GNT0	GNT1	LPC	0	0	PCI	0	1	*SPI	1	1		Inter Pu Hi
BOOT DEVICE	GNT0	GNT1													
LPC	0	0													
PCI	0	1													
*SPI	1	1													
PGNT-2	(inter pu)	*(-0),Desktop not pull low	DMI AC Coupling Low: Full Voltage Mode												
HDA_SDO	*POWERED BY EPW(-0)	POWERED BY CORE(inter pu)	NAND VCCQ PWR WELL SEL												
HDA_SYNC	*1.5V(-0)	1.8V	OD PLL VR SUPPLY SEL												
SPI_MOSI	*EN(-0)	DIS(inter pu)	TPM FUNCTIONALITY TPM DISABLED WHEN SAMPLED LOW												
NVR_ALE	*(10K)		DANBURY Technology Enable Enable When Sampled High												
NVR_CLE	*(-0)		DMI Termination Voltage DC Coup: TX/RX To VCC Is Sampled High												
INIT3_3V_N		*(-0)	Configurable CPU Output, Stronge This signal should not be pulled												
SPKR	*EN(1K)	DIS	STUFF TO ENABLE NO-REBOOT OPTION AT POWER-UP (CONFIGURATION STRAPPING).												
PCH_INTVRMEN	*EN(390K)		ENABLE INTERGRATED 1.05V SUS VRM.												
PCH_PU_GP33															
IGC_EN_N		*EN	INTEGRATED CLOCK CHIP ENABLE, Stuff Low For Full Clock Integration Enable.												
VCCVRM_EN	*EN(inter pu)	DIS(-0)	OD PLL VR(VccCLK,Vccap11EXP, VccFDIPLL,VccSATAPLL; DG P383)												
PCH_GP15	*EN(10K)	DIS	INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) WITH CONFIDENTIALITY												

CLOCK

SOURCE	DESCRIPTION

SIO H/W Monitor

FAN_TAC1	CPU_FAN
FAN_TAC2	SYS_FAN
FAN_CTL1	CPU_FAN
FAN_CTL2	SYS_FAN
TMPIN1	SYS_Temp
VIN0	+12V
VIN1	VCC
VIN2	VCORE
VIN4	CPUVTT
VIN5	V_DIMM
VIN6	V_1P05_PCH

PCI ROUTING

PCI1	AD17	INTA,B,C,D	PREQ-0	PGNT-0
PCI2	AD18	INTB,C,D,A	PREQ-1	PGNT-1
PCI3	AD19	INTC,D,A,B	PREQ-2	PGNT-2